In the Specification:

Please amend paragraph **[0014]** as follows:

[0014] Figs. 2A-2F are diagrams showing a cross-sectional view of a wafer which is processed ~~in accordance with~~ according to embodiments of the invention.

Please amend paragraph **[0015]** as follows:

[0015] Fig. 3 is a diagram showing a layout of a wafer in which the array area is isolated from the shining spot region at the edge of the wafer in accordance with embodiments of the invention.

Please add the following new paragraph after paragraph **[0015]**:

Figs. 4A-4E are diagrams showing a cross-sectional view of a wafer which is processed according to embodiments of the invention.

Please amend paragraph **[0018]** as follows:

[0018] Figs. 2A-2F illustrate the steps of a process according to embodiments of the invention.

Please amend paragraph **[0019]** as follows:

[0019] Fig. 2A shows a cross-section of a hard mask layer 202 that is formed atop a substrate 200 ~~(not shown)~~, which may be a pad nitride layer formed over a pad oxide layer and over a silicon substrate 200 as described above. A resist layer 204, such as a photoresist or other resist, is deposited atop the layer 202. Then, as Fig. 2C shows, a portion of the resist is exposed in a known manner, such as by transmitting light through one or more openings in a mask into a projection lens to focus a pattern onto the substrate 200. When the resist is a negative resist, the periphery region 204a is exposed so that the unexposed region 204b may be subsequently removed when the resist is developed. Alternatively, when the resist is a positive resist, the region 204b is exposed and is removed when the resist is developed so that only the periphery

region 204a remains. Fig. 2D illustrates the resist ring 206 that remains after the exposure and development steps.

Please insert the following new paragraph after paragraph **[0023]**:

An alternative embodiment of the invention is illustrated in Figure 4, which includes Figures 4A-4E. A pad oxide layer 301 is deposited atop the substrate 200, and a pad nitride layer 303 is deposited atop the pad oxide layer 301. A hard mask layer 202 is deposited atop the pad nitride layer 303, and a layer of resist 204 is deposited atop the hard mask layer 202 (Figure 4A). As illustrated now in Figure 4B, the layer of resist 204 is patterned to form a ring of resist 206 which separates a periphery of the substrate 200 from a further region of the substrate 200, thereby protecting devices formed in the further region of the substrate 200 from shining spots present in the periphery of the substrate 200. As illustrated in Figure 4C, a further layer of resist 208 is deposited atop the hard mask layer 202 and atop the ring of resist 206, and the further layer of resist 208 is patterned to form at least one patterned region 210 within the further region of the substrate 200 (Figure 4D). The ring of resist 206 is of sufficient thickness that a region of the further layer of resist 208 that is atop the ring of resist 206 is not patterned. The hard mask layer 202 is etched using the patterned further layer of resist 208 and the ring of resist 206 as an etch mask. As illustrated in Figure 4E, at least one trench region 320 in the substrate 200 is etched using the hard mask layer 202 and the ring of resist 206 as an etch mask. The ring of resist 206 is of sufficient thickness such that a region of the hard mask layer 202 that is beneath the ring of resist 206 remains after the trench region 320 is etched.